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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

THOMAS, TONIAE M

ART UNIT PAPER NUMBER

2822

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/942,907

Applicant(s)

IKURA, TSUNEO

Examiner

Toniae M. Thomas

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 October 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2-4, 7 and 9 is/are rejected.
- 7) ☒ Claim(s) 5, 6 and 8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

1. This Office action is an official response to the amendment filed on 09 October 2003.
2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.
3. Applicant's arguments, see page 4, lines 3-7 filed 09 October 2003, with respect to the rejection of claim 7 under 35 USC §102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Xing et al. (US 6,153,490). The indicated allowability of claim 3 is withdrawn in view of the newly discovered reference to Xing et al. (US 6,153,490). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3, 4, 7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xing et al. (US 6,153,490) in view of Tu et al. (US 6,627,493 B2) and Wolf (Silicon Processing for the VLSI Era - Vol. 2: Process Integration).

The Xing et al. patent (Xing) discloses a method for fabricating a semiconductor device (figs 9a-9i and col. 9, line 50 – col. 10, line 51). The method comprises the following steps: forming, on a substrate, a first insulating film 900 (fig. 9a and col. 9, lines 53-54); partially retaining the first insulating film in a first region through selective etching using a first mask pattern formed on the first insulating film (fig. 9a and col. 9, lines 55-56); forming a second insulating film 920 with a relatively high dielectric constant and high mechanical strength, such that the second insulating film covers the retained first insulating film (fig. 9g); forming a thinned portion of the second insulating film on the retained first insulating film by planarizing the second insulating film (col. 10, lines 39-40); forming a first interconnect groove 922 in the thinned portion of the second insulating film and the retained first insulating film through selective etching the thinned portion of the second insulating film and the retained first insulating film using a second mask pattern formed on the thinned portion of the second insulating film (fig. 9h and col. 10, lines 40-42); and forming a buried interconnect in the first interconnect groove, whereby the thinned portion of the second insulating film and the retained first insulating film are provided on the sides of the buried interconnect (fig. 9i).¹

¹ The buried interconnect comprises that portion of the bit line structure 96 that is formed within the interconnect groove 922. See also the Parekh et al. patent (US 5,981,333), figs. 13, 14 and col. 6, lines 28-42. Parekh describes a bit line structure, wherein the bit line structure comprises a buried interconnect 114 (i.e. the bit line contact) and a bit line 116. The bit line structure disclosed by Parekh is identical to the bit line structure disclosed by Xing.

Both the first insulating film and the second insulating film include inorganic materials as principal constituents (col. 9, lines 53-54 and col. 10, lines 39-40), and the step of forming the first interconnect groove includes a sub-step of forming a second interconnect groove in a second region, which is different from the first region, of the second insulating film through selective etching using the second mask pattern, as recited in claim 3 (fig. 9h).² A second interconnect groove is formed in a second region, which is different from the first region, of the second insulating film through selective etching using the second mask pattern *in forming an upper portion of the first interconnect groove in the thinned portion of the second insulating film* through the selective etching using the second mask pattern, as recited in claim 4 (fig. 9h).

Xing lacks anticipation in not teaching the following limitations: forming the first insulating layer 900 with a relatively low dielectric constant and low mechanical strength, as recited in claim 7; forming the thinned portion of the second dielectric film by polishing, as recited in claim 7; and forming the first insulating film 900 such that it includes an organic material as a principal constituent, as recited in claim 4.

The Tu et al. patent (Tu) discloses a method for forming a semiconductor device (figs. 1-8 and accompanying text), which is compatible with the method disclosed by Xing. The method comprises the steps of: forming, on a substrate, a first insulating film 20 with a relatively low dielectric constant and low mechanical strength (fig. 6 and col. 6, lines 41-50); and forming a second insulating film 24. In the instance wherein the first

² See also Appendix A.

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insulating film is a spin on polymer, the first insulating film 20 includes an organic material as a principle constituent.

Wolf (Vol. 2) describes the use of chemical mechanical polishing (CMP) as a planarization method (page 238, Section 4.4.11).

Since both Xing, Tu, and Wolf are from the same field of endeavor, the purposes disclosed in Tu and Wolf would have been recognized in the pertinent art of Xing by one having ordinary skill in the art at the time the invention was made.

One having ordinary skill in the art would have been motivated to modify Xing, at the time the invention was made, by forming the first insulating layer 900 of a material having a relatively low dielectric constant and low mechanical strength, wherein the first insulating film includes an organic material as a principal constituent, as taught by Tu, and forming the thinned portion of the second dielectric film by a polishing method, as taught by Wolf for the following reasons: forming the first insulating layer 900 of a material having a low dielectric constant lowers the capacitance between adjacent via contacts, and using CMP to planarize the second insulating layer 920 rapidly removes small elevated features without significantly thinning the second insulating layer on flat areas (Wolf - "Chemical Mechanical Polishing" page 238, first paragraph, lines 6-9).

5. *Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Xing, Tu, and Wolf as applied to claim 7 above, and further in view of Kawakubo et al. (US 6,165,837).*

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Xing does not teach forming, on the buried interconnect, a third insulating film for preventing diffusion of a metal included in the buried interconnect.

The Kawakubo et al. patent (Kawakubo) discloses a method for forming a semiconductor device (fig. 1B and accompanying text). The method comprises forming an insulating layer 20a over a bit line structure, which comprises a bit line contact 18a (i.e. buried interconnect) and a bit line 18 b (fig. 1B and col. 6, lines 18-26).

Since Xing and Kawakubo are all from the same field of endeavor, the purpose disclosed in Kawakubo would have been recognized in the pertinent art of Kawakubo at the time the invention was made by one having ordinary skill in the art.

Since the bit line structure of Xing comprises either polysilicon or tungsten, one having ordinary skill in the art would have been motivated to modify the combination of Xing, Tu, and Wolf, at the time the invention was made by forming a third insulating film on the bit line structure including the buried interconnect, as taught by Kawakubo, to prevent the diffusion of the material included in the buried interconnect into subsequently deposited layers.

Allowable Subject Matter

6. *Claims 5, 6, and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.*

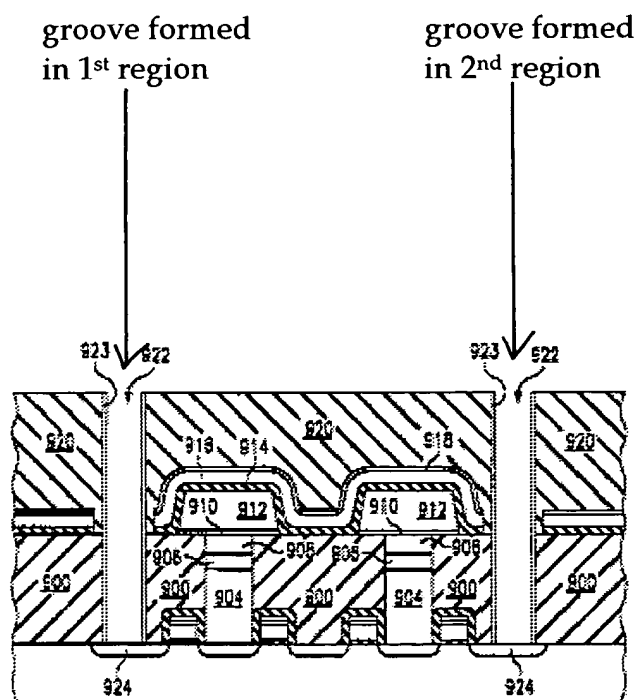
The prior art of record does not anticipate, teach, or suggest, either separately or combined, a method for forming a semiconductor device substantially as claimed,

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wherein the method comprises the following steps: removing the second mask pattern in forming a lower portion of the first interconnect groove in the first insulating film; forming the thinned portion of the second insulating film having a thickness of 10 nm through 50 nm;³ and forming the thinned portion of the second insulating film such that the thickness of the thinned portion in the first region is smaller than a thickness of the second insulating film in a second region.

³ The thinned portion of the second insulating film 920 has a thickness of 500nm (Xing - col. 10, lines 39-40), which is much thicker than the claimed range of 10-50 nm. There is no motivation or suggestion to modify Xing by forming the second insulating film to a thickness of only 10-50 nm.

Appendix A



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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (703) 305-7646. The examiner can normally be reached on Monday through Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JMJ

06 November 2003


AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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